Please type a plus sign (+) inside this box → +

HDP/SB/21 based on PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/779,677
Filing Date	February 18, 2004
Inventor(s)	Dae-Seung JEONG et al.
Group Art Unit	2611
Examiner Name	Timory A. Kabir
Attorney Docket Number	9862-000017/US

ENCLOSURES *(check all that apply)*

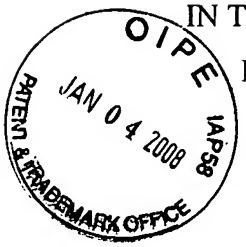
- ☐ Fee Transmittal Form
- ☒ Fee Attached
- ☐ Amendment
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Letter to the Official Draftsperson and _____ Sheets of Formal Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ LETTER SUBMITTING APPEAL BRIEF AND APPEAL BRIEF (w/clean version of pending claims)
- ☒ Appeal Communication to Group *(Notice of Appeal, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

Attn: Mail Stop BPAI

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name John A. Castellano	Reg. No. 35,094
Signature			
Date	January 4, 2008		



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:

Dae-Seung Jeong, et al.

Application No.: 10/779,677 Examiner: Timory A. Kabir

Filed: February 18, 2004 Docket No.: 9862-000017/US

For: RECOVERY OF CLOCK AND DATA USING QUADRATURE CLOCK SIGNALS

BRIEF ON APPEAL

01/07/2008 MAHMED1 00000108 10779677

01 FC:1402 510.00 OP

Appeal from Group 2611

Harness, Dickey & Pierce, PLC
11730 Plaza America Drive, Suite 600
Reston, VA 20190

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST 3
II. STATEMENT OF RELATED APPEALS AND INTERFERENCES 4
III. STATUS OF CLAIMS 5
IV. STATUS OF AMENDMENTS 6
V. SUMMARY OF CLAIMED SUBJECT MATTER 7
VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL 9
VII. ARGUMENTS 10
A. Claims 1-17 and 21-23 Are Not Anticipated By Izzard 10
B. Claims 18-20 Are Not Obvious Over The Combination of Izzard and Savoj 11
a. Improper Rejection 12
b. Failure to Disclose Claimed Elements 12
c. Improper Claim Interpretation 13
VIII. CONCLUSION 15
Appendix A 16
Appendix B 21
Appendix C 22

I. REAL PARTY IN INTEREST

The real party in interest for this appeal and the present application is SAMSUNG ELECTRONICS CO., LTD., by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 014997, Frame 0855.

II. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences, or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon the Board's decision in the pending Appeal.

IV. STATUS OF AMENDMENTS

No amendments have been made to the pending claims during prosecution of the present application. Arguments were submitted on May 18, 2007, in response to the first Office Action mailed on February 21, 2007. A second and Final Office Action was issued on August 6, 2007. This Appeal is from the Final Rejection of the pending claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter of the present application relates to a clock and data recovery (CDR) circuit for use in data networking. Data receiving devices (bridges, routers, switches, etc.) in data networks must clear up or re-time distorted data. A CDR may be used to perform such tasks. A CDR receives distorted data, and provides a CLOCK signal and re-times (or recovers) data as outputs. In an example embodiment of the subject matter of the present application, the CDR may be a phase-locked loop and include a quarter-rate phase detector.

Independent claim 1 describes, a quarter-rate phase detector (210; Fig. 2) comprising:

four latches (301-304; Fig. 3A; [0023]) controllable to latch, at different times according to quadrature clock signals (I, IB, Q, QB; Fig. 3A; [0021]), respectively, data (D_{IN}; Figs. 2, 3A) received by the phase detector so as to form latched signals (m1-m4; Fig. 3A; [0024]);

an error circuit (318; Fig. 3A; [0024]) to combine corresponding ones of the latched signals, respectively, resulting in a plurality of intermediate signals (E1-E4; Fig. 3A; [0025]); and

a multiplexing unit (316; Fig. 3A; [0025]) to selectively output the intermediate signals as a phase error signal (E, EB; Figs. 2, 3A, 3D; [0027]).

Independent claim 14 describes a quarter-rate phase detector (210; Fig. 2) comprising:

four data latches (301-304; Fig. 3A; [0023]), each latch receiving the same input data (D_{IN}; Figs. 2, 3A), the latches being clocked by quadrature clock signals (I, IB, Q, QB; Fig. 3A; [0021]), respectively, so as to produce latched signals (m1-m4; Fig. 3A; [0024]); and

an error signal-generating circuit (318; Fig. 3A; [0024]) to generate a phase error signal (E, EB; Figs. 2, 3A, 3D; [0027]) based upon the four latched signals and the quadrature clocks signals.

Independent claim 16 describes a quarter-rate phase detector (210; Fig. 2) comprising:

four XOR gates (309-312; Fig. 3A; [0024]) receiving latched signals (m1-m4; Fig. 3A; [0024]), each latched signal corresponding to input data (D_{IN}; Figs. 2, 3A) latched according to one of quadrature clock signals (I, IB, Q, QB; Fig. 3A; [0021]), respectively, each XOR gate generating an intermediate signal (E1-E4; Fig. 3A; [0025]);

a multiplexer (316; Fig. 3A; [0025]) to selectively output one of the four intermediate signals as a phase error signal (E, EB; Figs. 2, 3A, 3D; [0027]).

Independent claim 18 describes a clock and data recovery (CDR) circuit (200; Fig. 2; [0019]) comprising:

a phase-error generating circuit to determine quarter-rate phase detector (210; Fig. 2; [0019]-[0020]);

a charge pump (220; Fig. 2; [0019] operable upon an output of the phase detector (Fig. 2; [0020];

a filter (230; Fig. 2) operable upon an output of the charge pump (Fig. 2; [0020]); and

a quadrature voltage-controlled oscillator (VCO) (240; Fig. 2) operable upon an output of the filter (Fig. 2; [0020]);

the phase-detector being controllable by the output of the VCO (Fig. 2; [0020]).

Independent claim 21 describes a method of detecting phase at a quarter of the rate of the received data (Figs. 2, 3A), the method comprising:

latching, at different times according to quadrature clock signals, respectively, the received data so as to form latched signals (Figs. 2, 3A; [0021]-[0024);

combining corresponding ones of the latched signals, respectively, to provide a plurality of intermediate signals (Fig. 3A; [0024]-[0025]); and

selectively outputting one among the intermediate signals, respectively, to provide a constructed a phase error signal (Figs. 2, 3A-3D; [0025]-[0027]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

1) Claims 1-17 and 21-23 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,506,874 to Izzard, et al. (Izzard).
2) Claims 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Izzard in view of U.S. Patent 6,847,789 to Savoj, et al. (Savoj).

VII. ARGUMENTS

A. Claims 1-17 and 21-23 Are Not Anticipated By Izzard.

Claims 1-17 and 21-23 stand rejected under 35 U.S.C. §102(b) as being anticipated by Izzard. Under 35 U.S.C. §102(b) a person shall be entitled to a patent unless the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.

It is alleged in the Final Office Action that Izzard anticipates claims 1-17 and 21-23 because Izzard discloses each and every feature recited in the rejected claims. However, Izzard fails to disclose "four latches controllable to latch, at different times according to quadrature clock signals," as recited in independent claim 1; "data latches, the latches being clocked by quadrature clock signals," as recited in independent claim 14; "four XOR gates receiving latched signals, which are latched according to one of quadrature clock signals," as recited in claim 16; and a method of detecting phase at a quarter of the rate of the received data, including "latching, at different times according to quadrature clock signals," as recited in independent claim 21.

Izzard relates to a data re-timing circuit and specifically to a phase detector that can be used with a half-baud dock and serial data (column 1, lines 5-7). Izzard describes a phase detector and method that use a series of latches and quadrature clock signals. However, as clearly shown in Fig. 1 of Izzard, the quadrature clock signals I and Q are not used to control the latching of latches, but rather are used for data inputs to the latches. Izzard explicitly recites, "[I]nput signal I is applied to the input of latch 12 and of latch 14. Latch 12 generates sampled clock I' *when the signal D is applied to clocking input CLK is low* but holds input I *when the signal applied to clocking input CLK is high* (emphasis added) (column 2, lines 54-57). Thus, according to Izzard, it is the clock signal D that controls latching and not by signals I, Q that are in quadrature.

Izzard also discloses that "input signal Q is applied to the input latch of 16 and also to the input latch of 18. Latch 16 works in the same manner as latch 12 and latch 18 works

in the same manner as latch 14" (column 2, lines 63-66). Izzard also clearly states that signal D is not a quadrature clock signal, but rather is "an arbitrary stream of digital signals" (column 3, lines 25-28). Thus, as in clearly disclosed in Izzard, the latching of the latches in the arrangement of Izzard is controlled by a data signal D which is fed into the clocking input of each latch as shown in Figs. 1 and 9.

It is also alleged in the Office Action that the latches 12a, 12b, 16a, 16b of Fig. 9 are four latches controllable to latch at different times according to quadrature clock signals, respectively, data received by the phase detector. However, the latches of Izzard are controlled by the signal D and not a quadrature clock signal. As clearly stated in Izzard, the input signals I, Q are used as data inputs to the latches. For example, as shown in Fig. 9 of Izzard, the signal CLK1 and CLK2 equal the input signal I each of which are fed into the data inputs of the latches 12a and 12b.

Similarly, the signals Mark 1 and Mark 2 correspond to Q signals and are fed into the data inputs of latches 16a and 16b (see Fig. 9; column 5, lines 33-38). Moreover, as clearly shown in Fig. 9, the D signal is fed into the clock port of all of the latches and as such the latches are controlled according to the D signal and not quadrature clock signals.

B. Claims 18-20 Are Not Obvious Over The Combination of Izzard and Savoj.

Claims 18-20 stand rejected under 35 U.S.C. §103(a) as being rendered obvious by the combination of Izzard and Savoj. According to 35 U.S.C §103(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between subject matter sought to be patented in the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

It is alleged in the Final Office Action that claims 18-20 are unpatentable over the combination Izzard and Savoj. However, the combination of references fails to disclose or suggest the "phase detector being controllable by the output of the VCO" (voltage controlled oscillator).

a. Improper Rejection

Although it is alleged in the Final Office Action that a phase detector being controllable by the out of the VCO is disclosed in Izzard, no corresponding structure is identified to support the allegation. When indicating that a rejection is under 35 U.S.C. §103, the Examiner should set forth in the Office Action (a) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page numbers and line numbers where appropriate; (b) the difference or differences in the claim over the applied references; (c) a proposed modification of the applied reference if necessary to arrive at the claimed subject matter; and (d) an explanation of why one of ordinary skill in the art at the time of the invention was made would have been motivated to make the proposed modification. Further, in rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified (37 CFR §1.104, MPEP 706.02(j)).

As no corresponding structure is identified, a *prima facie* case of obviousness has not been established and therefore, the rejection is improper.

b. Failure To Disclose Claimed Elements

Additionally, although not properly identified in the Final Office Action, Izzard discloses a phase detector 10 and voltage controlled oscillator (VCO) 38 at Fig. 11. Izzard states that "the output of VCO 38 is the clocking signal I" (i.e., quadrature clocking signal I) [column 6, lines 23-24]. As described above, and clearly established in Izzard, the quadrature clocking signal I does not control the phase detector 10, but rather, I is used as a data input to one or several of the latches of the phase detector 10, as shown in FIG. 1 of Izzard. Thus, the phase detector 10 of Izzard is not controllable by the output of the VCO 38. Rather, the signal D controls the phase detector by controlling the latching of the latches in the arrangement according to Izzard, and signal D is not the output of VCO 38.

In the Final Office Action, Savoj is combined with Izzard for allegedly teaching a "charge pump" that is admitted as being deficient from the Izzard reference. However, even

were the combination of references made as proposed in the Final Office Action, because Savoj fails to disclose or suggest a phase detector being controllable by the output of the VCO, Savoj fails to overcome the deficiencies of Izzard. Thus, the combination of references fails to render the rejected claims obvious.

c. Improper Claim Interpretation

In the Response to Arguments section of the Final Office Action, it is alleged that: "the Examiner is entitled to give the broadest reasonable interpretation to the language of the claim. So the Examiner considers 'I and Q signals in figure 11' are 'controlling the phase detector' within the broad meaning of the term. The Examiner is not limited to Applicant's definition, which is not specifically set forth in the claims."

Appellants respectfully submit that during examination, "claims yet unpatented are to be given broadest reasonable interpretation consistent with specifications during examination of a patent application" *In re Prater*, 415 F.2d 1493 (1969) (MPEP §2111). Thus, the Examiner's belief that he is "entitled to give the broadest reasonable interpretation of the language of the claim" is correct only so long as that "reasonable interpretation is "consistent with the specification."

In the present case, it is clear from a reading of the claims and specification that the output of the VCO 240 are quadrature clock signals I, IB, Q, QB, and that it is those quadrature clock signals that control the phase detector 210. In contrast, the quadrature signal I in Izzard does not control the phase detector 10, but rather are merely data inputs (Fig. 1, 9 of Izzard).

Moreover, interpreting a prior art reference, the Examiner must consider the reference as a whole and in a manner consistent with the teachings of the reference. Thus, when interpreting Fig. 11 of Izzard, the Examiner must interpret the figure, and the disclosed elements, as taught by Izzard and not in a manner that the Examiner deems a "reasonably broad interpretation." Thus, interpreting the quadrature signal I of Izzard to control the phase detector is in direct conflict of Izzard in that Izzard specifically recites that the signal I is a data signal. It is further stated in Izzard that latching is controlled by the signal CLK (D) as shown in Figs. 1

and 9. Thus, the Examiner's claim interpretation is inconsistent with the MPEP and established case law.

VIII. CONCLUSION

For all of the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-23 are in condition for allowance. For all of the above reasons, Appellants respectfully request this Honorable Board to reverse the rejection of claims 1-23 and allow all pending claims.

Respectfully submitted,
HARNESS, DICKEY & PIERCE, P.L.C.

By: _____
John A. Castellano, Reg. No. 35,094

APPENDIX A – CLAIMS APPENDIX

1. A quarter-rate phase detector comprising:

four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals;

an error circuit to combine corresponding ones of the latched signals, respectively, resulting in a plurality of intermediate signals; and

a multiplexing unit to selectively output the intermediate signals as a phase error signal.

2. The quarter-rate phase detector of claim 1, wherein:

the quadrature clock signals include signals I, Q, Ib and Qb;

a first one of the latches is controlled by I;

a second one of the latches is controlled by Q;

a third one of the latches controlled by Ib; and

a fourth one of the latches is controlled by Qb.

3. The quarter-rate phase detector of claim 1, wherein the multiplexing unit is controllable by the quadrature clock signals.

4. The quarter-rate phase detector of claim 1, wherein the multiplexing unit is controllable to truncate the intermediate signals.

5. The quarter-rate phase detector of claim 4, wherein the multiplexing unit is operable to form the phase error signal by cycling through the truncated intermediate signals.

6. The quarter-rate phase detector of claim 1, wherein:

the quadrature clock signals include signals I and Q; and

the multiplexing unit is controlled according to the signals I and Q, respectively.

7. The quarter-rate phase detector of claim 6, wherein the multiplexing unit includes:

a first multiplexer and a second multiplexer to receive the intermediate signals, respectively; and

a third multiplexer to multiplex outputs of the first and second multiplexers.

8. The quarter-rate phase detector of claim 1, wherein

the corresponding latched signals are pairs of latched signals; and

each pair has a first set and a second set, the second set representing the latched signals subsequently closest in time to the first set, respectively.

9. The quarter-rate phase detector of claim 8, wherein:

the error circuit includes four exclusive OR (XOR) gates, each XOR gate receiving one of the pairs, respectively.

10. The quarter-rate phase detector of claim 1, wherein:

the four latches represent a first set of latches and the latched signals represent a first set of latched signals;

the detector further comprises:

a second set of four latches arranged to receive the outputs of the first set of latches, respectively, and controllable to latch data at different times according to the quadrature clock signals, respectively, so as to form a second set of latched signals; and

the second set representing re-timed versions of the received data.

11. The quarter-rate phase detector of claim 10, wherein:

the second set of latched signals is organized as pairs;

the detector further comprises:

a reference circuit to generate a reference signal based upon transitions in the second set of latched signals.

12. The quarter-rate phase detector of claim 11, wherein:

the second set of latched signals is organized as pairs;

the reference circuit includes:

a plurality of multiplexers to selectively output the pairs of re-timed data; and

an exclusive OR (XOR) gate to receive the outputs of the plurality of multiplexers.

13. The quarter-rate phase detector of claim 1, wherein the rate of the intermediate signals is ¼ of the received data rate.

14. A quarter-rate phase detector comprising:

four data latches, each latch receiving the same input data, the latches being clocked by quadrature clock signals, respectively, so as to produce latched signals; and

an error signal-generating circuit to generate a phase error signal based upon the four latched signals and the quadrature clocks signals.

15. The quarter-rate phase detector of claim 14, wherein the error-signal-generating circuit is operable upon the four latched signals and is controlled by the quadrature clocks signals.

16. A quarter-rate phase detector comprising:

four XOR gates receiving latched signals, each latched signal corresponding to input data latched according to one of quadrature clock signals, respectively, each XOR gate generating an intermediate signal;

a multiplexer to selectively output one of the four intermediate signals as a phase error signal.

17. The quarter-rate phase detector of claim 16, further comprising:

four data latches, each latch receiving the same input data, the latches being clocked by quadrature clock signals, respectively, so as to produce quadrature latched data signals;

18. A clock and data recovery (CDR) circuit comprising:

a phase-error generating circuit to determine quarter-rate phase detector;

a charge pump operable upon an output of the phase detector;

a filter operable upon an output of the charge pump; and

a quadrature voltage-controlled oscillator (VCO) operable upon an output of the filter;

the phase-detector being controllable by the output of the VCO.

19. The CDR circuit of claim 18, wherein the rate of the quadrature signals of VCO is ¼ of the received data rate of the phase-error generating circuit.

20. The CDR circuit of claim 18, wherein the phase-error-generating circuit includes:

four latches controllable to latch, at different times according to quadrature clock signals, respectively, data received by the phase detector so as to form latched signals;

an error circuit to combine corresponding ones of the latched signals, respectively, the error circuit providing a plurality of intermediate signals; and

a multiplexing unit to selectively output the intermediate signals as a phase error signal.

21. A method of detecting phase at a quarter of the rate of the received data, the method comprising:

latching, at different times according to quadrature clock signals, respectively, the received data so as to form latched signals;

combining corresponding ones of the latched signals, respectively, to provide a plurality of intermediate signals; and

selectively outputting one among the intermediate signals, respectively, to provide a constructed a phase error signal.

22. The method of claim 21, wherein:

the quadrature clock signals include signals I and Q; and

the selectively outputting step selectively outputs according to the signals I and Q, respectively.

23. The CDR circuit of claim 21, wherein the rate of the quadrature clock signals is ¼ of the received data rate.

APPENDIX B – EVIDENCE APPENDIX

None

APPENDIX C – RELATED PROCEEDINGS APPENDIX

None